2
FUNDAMENTALS OF ACTIVE DEVICES*

An active device is one that is capable of amplifying a signal. Accordingly, vacuum tubes, transistors, field-effect transistors, and linear integrated circuits are active devices, whereas resistors, capacitors, inductors, and transformers are passive devices.

Speaking more precisely, an active device must be able to increase the power level of an input signal. A step-up transformer will output a greater voltage than that applied to its input, but a transformer cannot have an output power greater than the input power. Hence, a transformer is not an active device.

In this chapter we present the fundamental principles of four types of active devices: bipolar junction transistors (BJTs), junction field-effect transistors (JFETs), insulated-gate field-effect transistors (MOSFETs), and vacuum triodes. Additionally, we briefly describe a general-purpose operational amplifier (op amp). We begin with a discussion of the physical principles of solid-state devices.

2-1 INTRINSIC SEMICONDUCTORS

The two most important semiconductor materials are silicon and germanium. The properties of the two are similar because atoms of each have four electrons in the outer shell. The outermost electrons are called *valence* electrons.

Considering that the nucleus and the inner electrons play only passive roles in determining the electronic properties of these materials, it is convenient to speak of a silicon *core* or a germanium *core* when referring to the nucleus and inner electrons. Hence, we may visualize a silicon or germanium atom as a core surrounded by four electrons. This picture emphasizes the importance of the four outer electrons.

The crystal structure of silicon and germanium easily accommodates four electrons in the vicinity of each atomic core. However, the electrons that occupy these positions belong more to the electronic structure of the crystal than to individual atoms, even though the electrons were carried into the structure by individual atoms. Each core, taken by itself, contains four positive charges (protons) that are not balanced with negative electrons. Hence, four electrons per core are required to establish electrical neutrality, and these electrons are provided by the electronic

* This material is from C. Green, *Technical Physics* (Englewood Cliffs, N.J.: Prentice-Hall, 1984).

structure of the crystal. Figure 2-1 is a two-dimensional representation of a silicon or germanium crystal.

Because silicon has far better properties than germanium for use in electronics, it is now, by far, the most popular semiconductor material. In the following we refer only to silicon, but the principles involved apply also to germanium.

Electron-Hole Pairs

The valence electrons gain energy as the material becomes warmer, and when an electron accumulates about 1.1 eV of thermal energy (for silicon), it is able to break away from its core and become free. We say the electron is *excited* from the *valence band* (of energy) into the *conduction band*. This produces a free electron (the one that was excited) and also a vacancy in the electronic structure where the electron originally resided. The vacancy is called a *hole*. Obviously, a hole is produced each time a free electron is produced, and we therefore speak of *thermally induced electron-hole pairs*. The word *pair*, however, does not imply that the free electron and hole stay together or even near each other after they are produced.

For temperatures above absolute zero, there will exist an equilibrium number of electron-hole pairs in an intrinsic semiconductor. At higher temperatures, the number increases. The presence of the free electrons and holes enables the semiconductor to conduct an electric current because mobile, charged particles are available to form the current. Furthermore, because more electron-hole pairs are present at higher temperatures, the electrical conductivity increases with temperature; warm semiconductors conduct better than cool semiconductors.

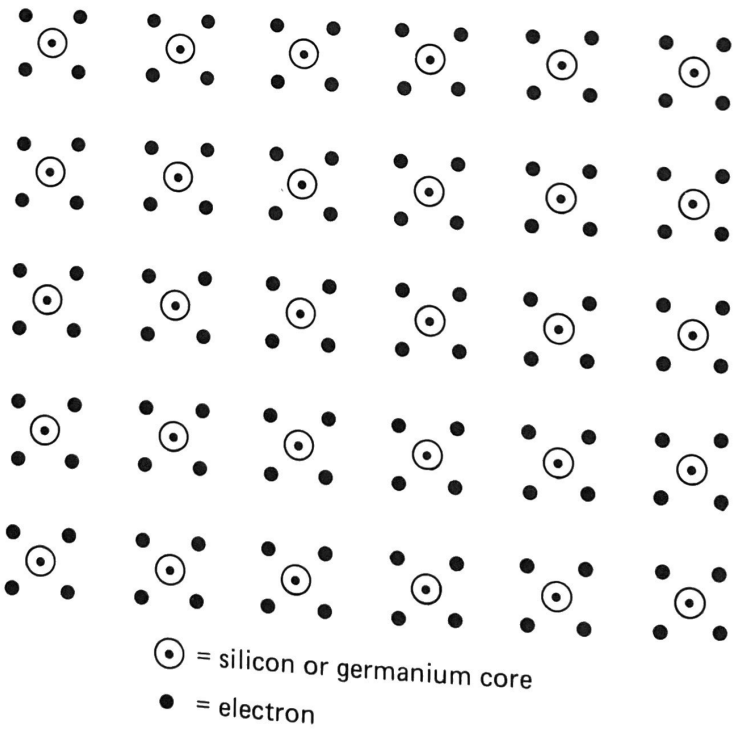


FIGURE 2-1 Two-dimensional representation of a silicon or germanium crystal. The electronic structure easily accommodates four electrons near each core.

Hole Conduction

It is easy to understand that the presence of free electrons in a silicon crystal will increase its conductivity, but it is somewhat surprising to find that the holes also increase the conductivity. That is, a hole can act as a charge carrier.

Recall that a hole is a vacancy, a place in the electronic structure where an electron could be but is not. But a hole in conjunction with a silicon core represents an imbalance of electrical charge. The hole-core combination appears positive because of the electron deficiency represented by the hole. The positive charge actually resides in the nucleus of the silicon atom, but it is convenient (and only slightly misleading) to speak of a hole as being positively charged an amount equal to the charge of one proton.

The mechanism of hole conduction is illustrated in Figure 2-2. A hole moves from one core to an adjacent core via an electron jump from one core to the other in the direction opposite to the motion of the hole. Motion of the hole to the left, from core 10 to core 1, is accomplished by successive electron jumps from 9 to 10, then from 8 to 9, and so on. The net result is a transfer of one negative charge from core 1 to core 10. Far less energy is required for an electron to move from a given core to a hole on an adjacent core than is required to excite the same electron to the realm of free electrons (into the conduction band).

2-2 DOPING—ADDING IMPURITIES TO SEMICONDUCTORS

Pure (intrinsic) semiconductors as such are not very useful because they are rather good insulators. The electrical conductivity of semiconductors can be increased dramatically, however, by the addition of minute quantities of selected impurities

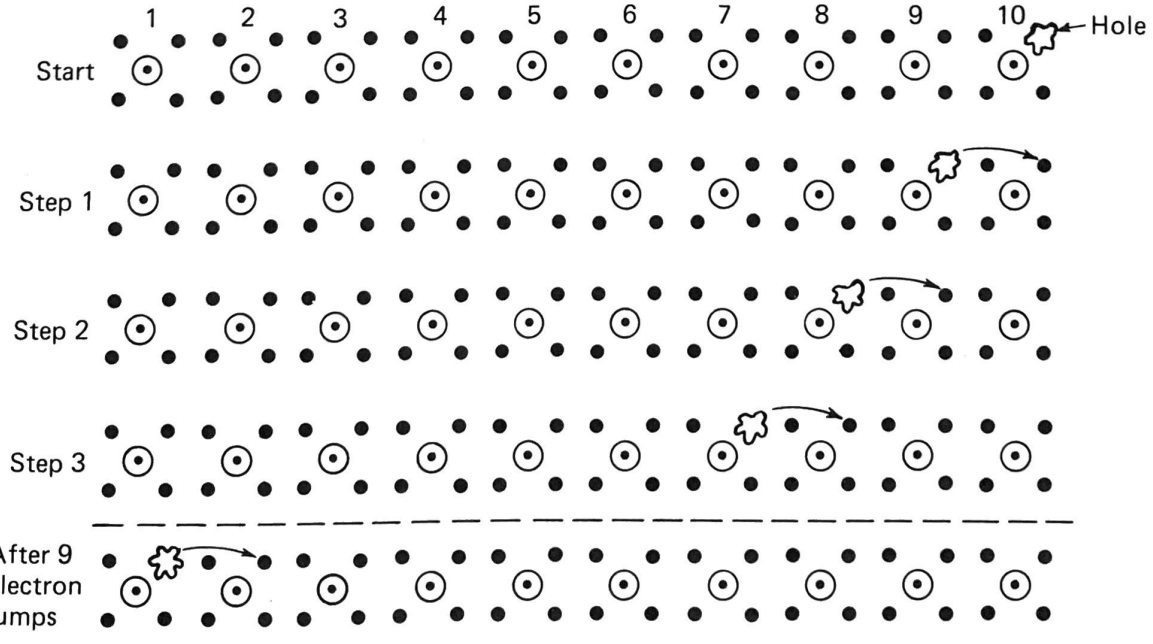


FIGURE 2-2 Illustration of hole motion along a line of silicon atoms. The hole moves to the left as electrons jump to the right.

to the semiconductor crystal. This process is called *doping*, and it serves to introduce either free electrons or free holes into the crystal, depending upon which dopant is used. An impurity concentration on the order of one part per million can result in a millionfold increase in the electrical conductivity of the material.

N-type Material

The elements phosphorus, arsenic, antimony, and bismuth consist of atoms that have five electrons in the outer shell. If one of these elements is used to dope a silicon crystal, a small number of the silicon atoms will be replaced by the impurity atoms. Since the impurity atoms have five electrons in the outer shell and since the electronic structure of the crystal easily accommodates only four electrons per core, the extra electron does not fit conveniently into the electronic structure of the crystal. But it must accompany the impurity atom into the crystal in order for the impurity atom to remain electrically neutral. The result is that the fifth electron is not as tightly bound to the atomic cores as are the four electrons that are easily accommodated. The fifth electron becomes a free electron (at ordinary temperatures) that can move under the influence of an electric field and form an electric current.

Semiconductors doped with impurities that contribute extra electrons are called *N-type semiconductors* because the polarity of the mobile charge carriers (the free electrons) is negative. Similarly, the impurities that produce *N*-type semiconductors are known as *N-type impurities*.

P-type Material

The elements aluminum, boron, gallium, and indium have only three electrons in the outer shell. When these elements are added as impurities to a semiconductor, each impurity atom contributes only three electrons instead of four to the electronic structure of the crystal. Thus, a hole exists at the site of each impurity atom. At ordinary temperatures, the holes become free holes and serve to increase the conductivity of the crystal.

Semiconductors doped with impurities that produce holes are called *P-type semiconductors*, and the impurities are called *P-type impurities*. The polarity of charge carriers in *P*-type materials (holes) is positive. A symbolic representation of *N*-type and *P*-type semiconductors is shown in Figure 2-3.

Current Conduction in Semiconductors

We have now described three types of semiconductors, intrinsic, *N*-type, and *P*-type. In intrinsic (undoped) semiconductors, current flow results from the motion of both electrons and holes that stem from thermally induced electron-hole pairs. Holes move in one direction and electrons move in the other. In comparison with doped semiconductors, the conductivity of intrinsic material is very small.

In *N*-type material, the impurity atoms contribute large numbers of free electrons in addition to the thermally induced electron-hole pairs. Consequently, cur-

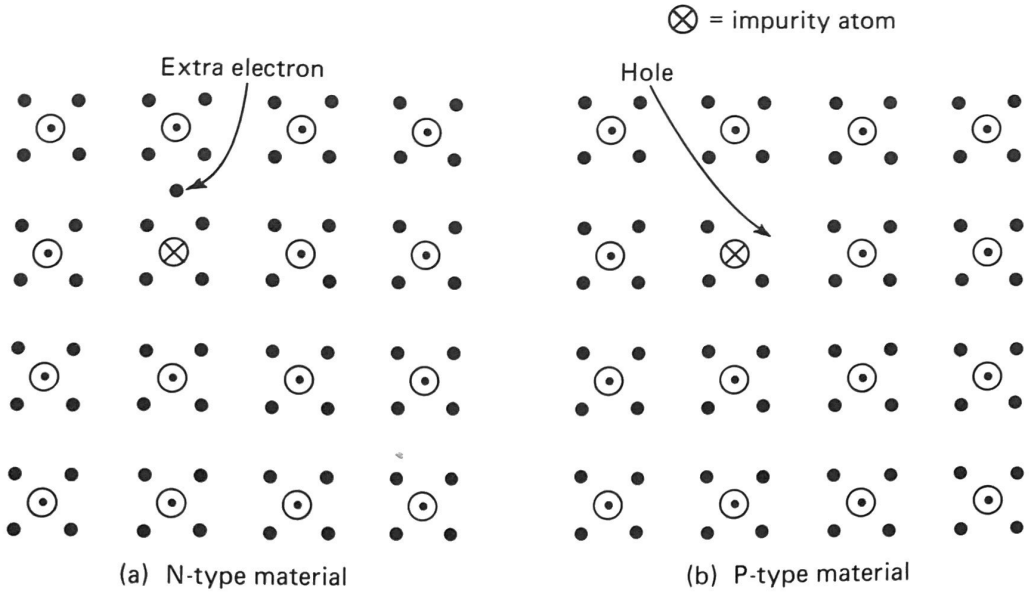


FIGURE 2-3 Representation of (a) *N*- and (b) *P*-type materials. The *N*-type impurity atom contributes an extra electron in *N*-type material, while the *P*-type impurity atom contributes a hole in the *P*-type material.

rent conduction is due primarily to the movement of free electrons. The thermally generated holes also contribute to the total current, but their effect is very small in comparison to that of the free electrons. In *N*-type material, the free electrons are the *majority carriers* while the holes are the *minority carriers*.

In *P*-type materials, free holes are the majority carriers. This is to say that current flow occurs primarily via the process of hole conduction. The thermally generated free electrons constitute the minority carriers.

We should always be mindful of the "nothingness" of holes. Hole conduction is actually caused by the movement of electrons in the opposite direction.

2-3 THE PN JUNCTION

A *PN junction* is formed where a region of *N*-type material is in intimate contact with a region of *P*-type material with the continuity of the crystal structure maintained at the interface between the two regions. Mechanically speaking, a dramatic change does not occur at the junction. The thing that changes, in crossing the junction, is the type of impurity atoms that are substituted for an occasional atom of the host material. Since the impurity concentrations are small, even this change is hardly noticeable, but the effect upon the electronic properties of the crystal is dramatic.

Suppose that a crystal of *N*-type material is suddenly joined to a crystal of *P*-type material, with the contact being such that the geometrical structures of the two crystals match up at the point of contact. The *N*-type material has an abundance of free electrons whereas the *P*-type material has an abundance of holes. When the two crystals are joined, what happens at the interface between the two types of material?

The obvious occurs. Free electrons near the interface on the *N*-side cross the interface and fill holes located near the interface on the *P*-side. The result is that free electrons of the *N*-type material disappear from the vicinity of the interface, and the holes near the interface on the *P*-side are filled by electrons coming over from the *N*-side. Thus, all charge carriers near the interface are *depleted*, and the region surrounding the interface, where there are neither electrons or holes, is called a *depletion layer*. This is illustrated in Figure 2-4.

The migration of free electrons across the interface does not continue until all free electrons in the *N*-material have gone over to fill the holes in the *P*-material. When an electron crosses from the *N*-side to the *P*-side, it leaves an unbalanced positive charge behind in the *N*-material and it contributes an extra negative charge to the *P*-material. A layer of positive charge develops near the interface in the *N*-material, and a layer of negative charge develops near the interface in the *P*-material. These layers establish an electric field across the interface that tends to oppose further migration of electrons. This limits the depletion layer thickness to values that are extremely thin in comparison to the overall dimensions of the *N*- and *P*-regions.

The depletion layer has no free electrons or holes, which makes it a good insulator. Thus, the depletion layer represents a layer of insulation that naturally develops between the *N*- and *P*-regions. In the following, however, we shall see that the thickness of this layer may be altered by applying an external voltage to the *N*- and *P*-regions. We shall see that electrons will flow across the junction in one direction but not the other. That is, a *PN* junction exhibits the properties of a *rectifier*.

Forward-Biased PN Junction

In Figure 2-5(a), a voltage source is connected to a *PN* junction with the positive voltage applied to the *P*-type material. Holes are repelled from the positive terminal through the *P*-region toward the interface. On the other side, electrons are repelled from the negative terminal through the *N*-region toward the interface. The result is that the depletion layer becomes narrower, and when the applied voltage reaches about 0.6 V, the depletion layer practically disappears and a comparatively large current will flow across the junction and through the external circuit. Under this condition, the junction is said to be *forward-biased*.

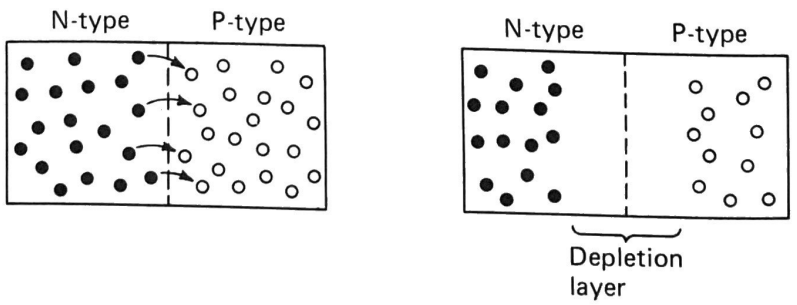


FIGURE 2-4 Formation of the depletion layer at the interface of a *PN* junction. Electrons cross the interface from the *N*-material to fill holes near the interface in the *P*-material.

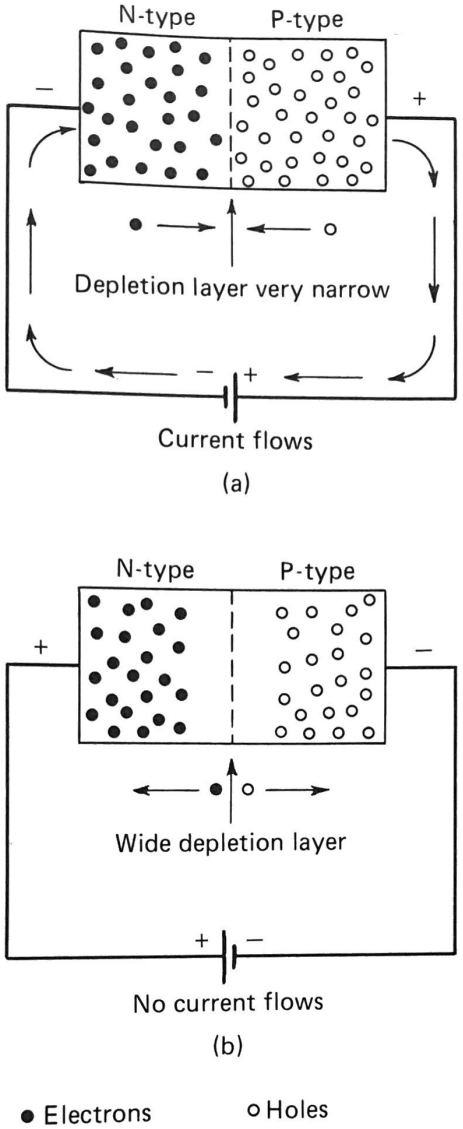


FIGURE 2-5 (a) Forward-biased and (b) reverse-biased PN junction.

Electron flow through the *N*-material of a forward-biased *PN* junction is by the movement of free electrons through the crystal toward the interface. At the interface, the electrons combine with holes arriving at the interface from the other direction. In the *P*-material, conduction is by the movement of holes in the manner depicted in Figure 2-2.

Reverse-Biased PN Junction

In Figure 2-5(b), the external voltage is connected with the positive voltage applied to the *N*-type material. Free electrons are attracted to the positive terminal and are drawn through the *N*-material away from the interface. On the other side, holes are attracted to the negative terminal and are also drawn away from the interface. The result is that the depletion layer becomes wider; no current flows

across the junction due to the absence of mobile charge carriers in the depletion layer. Under this condition, the junction is said to be *reverse-biased*.

Conduction Characteristics of PN Junction

The forward-and-reverse conduction characteristics of a *PN* junction are shown in Figure 2-6. Current flow is plotted along the vertical axis and the applied voltage is plotted along the horizontal axis. The right-hand side of the graph is the region of forward bias; the reverse-bias region is on the left.

As the applied voltage is increased from zero in the direction of foward bias, the current increases very slowly (actually exponentially) until a forward bias of about 0.5 V is reached. The current then increases more rapidly, and the plot turns upward sharply at about 0.65 V. The region where the plot turns upward is called the *knee* of the curve. Beyond about 0.7 V, the current increases dramatically as the applied voltage is increased.

The reverse characteristic is obtained by reversing the polarity of the voltage applied to the junction. As the reverse voltage is increased, a very small *saturation current*, I_s, begins to flow that remains essentially constant until the reverse voltage becomes quite large, perhaps several hundred volts. This saturation current is on the order of 10^{-12} A and is therefore negligible in most practical applications, because the forward current is typically on the order of 10^{-3} A or larger. As the reverse voltage is further increased, the *breakdown region* of the device is ap-

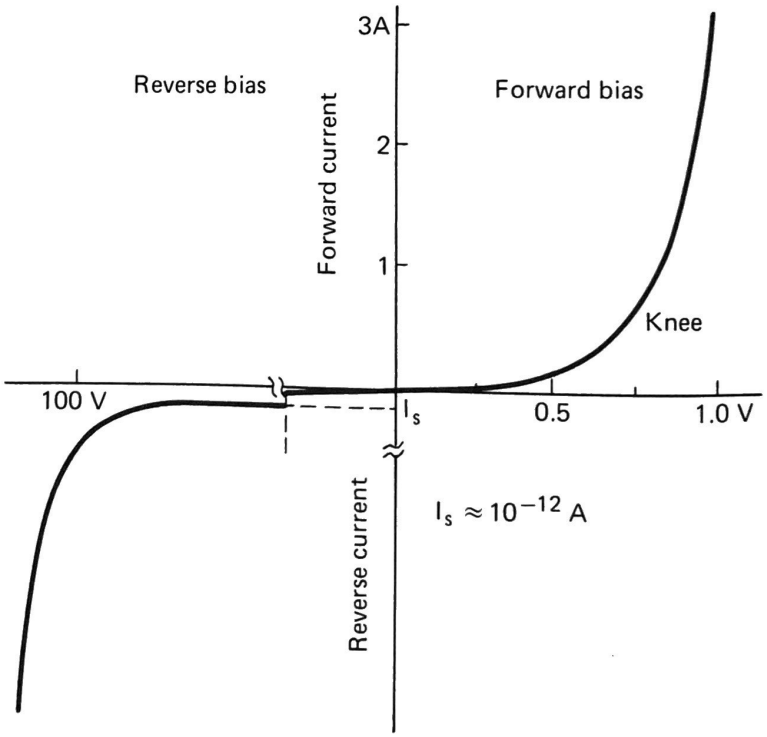


FIGURE 2-6 Forward- and reverse-conduction characteristic of a *PN* junction. Note that the scales are different in the forward and reverse regions.

proached, and it begins to conduct in the reverse direction. In practical applications, such as a rectifier, a *PN* junction (a *diode*) must not be allowed to enter the reverse breakdown region.

For voltages greater than about 100 mV applied in the forward direction, the current that will flow through a diode is given to a good approximation by

$$I = I_s e^{V_d/26} \tag{2-1}$$

for a silicon diode at room temperature. In this equation, V_d is the voltage applied to the diode (expressed in millivolts) and I_s is the saturation current. You may verify that when V_d is 700 mV and I_s is 10^{-12} A, the current I is 0.49 A.

2-4 SOLID-STATE DIODES

PN junctions are widely used in electronics and are known as *solid-state diodes* (to distinguish them from the now obsolete vacuum diodes). They serve many functions, one of which is as rectifying elements in power supplies that convert alternating current to direct current for use in TVs, radios, phonographs, and so forth.

Ordinary diodes intended for use in power supplies are characterized by two important parameters. One is the *maximum forward current*, which is the maximum current that the diode can safely conduct in the forward direction. The other is the *peak inverse voltage* (PIV), which is closely related to the reverse breakdown voltage of the junction. Inexpensive diodes may safely handle a current of 10 A while larger, more expensive units may handle currents in the hundreds of amps. PIVs may range from 50 V to 1000 V or more for diodes commonly encountered.

The schematic symbol for a solid-state diode and the direction of electron flow is shown in Figure 2-7.

Zener Diodes

A special class of solid-state diodes called *zener diodes* is fabricated so that the reverse-breakdown characteristic is very sharp and occurs at low voltages. These diodes are used as voltage regulators because the voltage developed across the diode in the reverse-breakdown region is essentially independent of the current

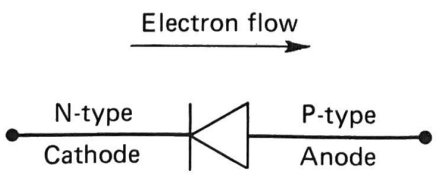


FIGURE 2-7 Symbol for a solid-state diode. Electrons flow from the cathode to the anode (terminology held over from the era of vacuum tubes).

flowing through the diode. The reverse conduction characteristic of a zener diode is shown in Figure 2-8(a) and a simple regulator circuit is shown in Figure 2-8(b). As voltage regulators, zeners are always operated in the reverse breakdown region. Zeners are characterized by their zener voltage V_z, and values of V_z range from slightly less than 3 V to 100 V or more.

As the source voltage in Figure 2-8(b) is increased from zero, the voltage across the zener increases linearly until V_z is approached. No current (practically speaking) flows through the zener until the vicinity of V_z is reached, and then the zener current increases sharply. At this point, voltage $V_s - V_z$ appears across the series resistor R_s. A further increase in V_s causes the voltage across the zener to increase only slightly, but the additional current increases the IR drop across R_s so that the voltage across the zener remains nearly equal to V_z.

Light-Emitting Diodes

These devices, known commonly as LEDs, are widely used as indicator and pilot lamps in a wide variety of electronic devices. The junction is designed so that light (usually red, green, or yellow) is produced when electrons combine with holes as

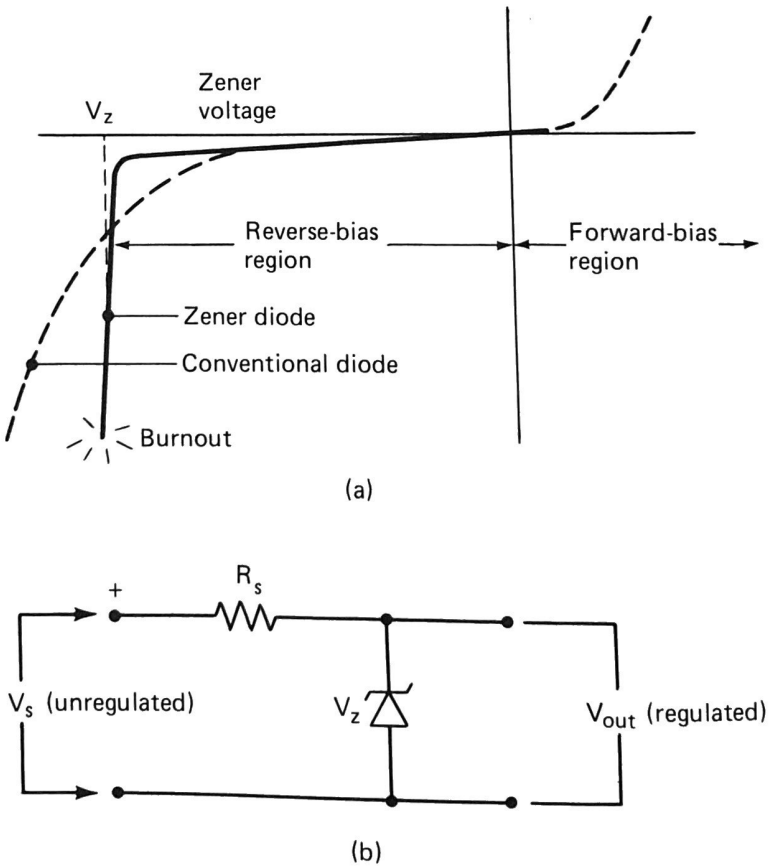


FIGURE 2-8 (a) The reverse breakdown characteristic of a zener diode is much sharper than that of a conventional diode. (b) Simple regulator circuit.

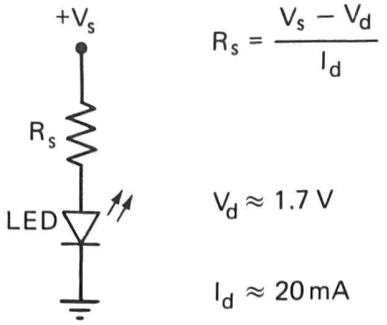


FIGURE 2-9 LED indicator circuit.

the junction conducts in the forward direction.* Typical junction currents range from 15 to 25 mA, and the voltage developed across the junction ranges from about 1.5 to 2.0 V. The junction voltage is higher than the familiar 0.7 V because a different semiconductor material (gallium arsenide, GAs) is used instead of silicon. The basic LED indicator circuit is shown in Figure 2-9. As for zener diodes, a series resistor must be included in order to limit the flow of current through the diode.

2-5 BIPOLAR JUNCTION TRANSISTORS

We now consider a solid-state device that is capable of amplification, the *biopolar junction transistor* (BJT). It is *bipolar* because both *N*- and *P*-type materials are used, and it is a *junction* transistor because two *PN* junctions form the heart of the device.

A BJT is a semiconductor sandwich consisting of a thin layer of *N*- or *P*-material sandwiched between two regions of material of the opposite type, as shown in Figure 2-10. Two possible configurations give rise to *NPN* and *PNP* transistors as shown. The terminals are identified as the emitter E, base B, and collector C, and we identify the junctions as the base-emitter (B-E) junction the base-collector (B-C) junction. We shall describe BJT operation in terms of an *NPN* silicon device.

Examine the circuit of Figure 2-11. Note that battery *A* forward biases the BE junction. Observe that switch *S* is open so that no external voltage is applied to the collector. When the voltage of *A* reaches the knee voltage of the junction, electrons will flow from the *N*-type emitter region into the *P*-type base region and out into the external circuit. The magnitude of the current depends upon the voltage applied to the junction by battery *A*, and a graph of the current vs. the applied voltage would resemble the forward conduction characteristic that is typical of *PN* junctions. When the voltage of *A* drops below the knee voltage (about 0.6 V for

* Because LEDs light up when they conduct, a vivid demonstration of the action of a bridge rectifier, for example, can be performed by using LEDs as rectifier diodes and then using a source of "slow AC" (about 1 Hz) to drive the bridge. The slow AC signal can be obtained from a function generator.

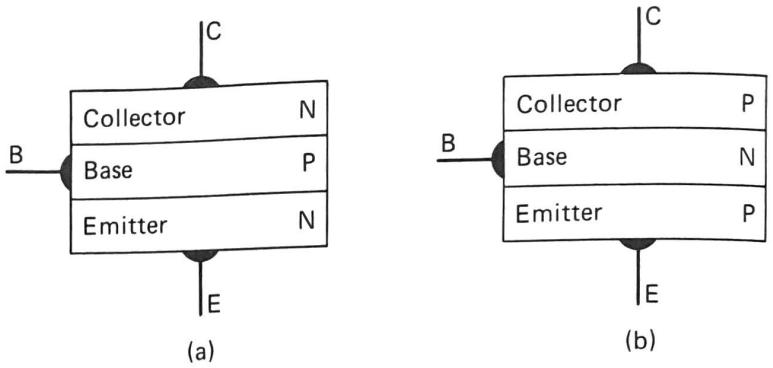


FIGURE 2-10 (a) *NPN* and (b) *PNP* bipolar junction transistors. Actual device geometries differ greatly from this simple pictorial representation.

silicon), electron flow into the base drops to very low levels. If the voltage of A were increased to about 0.9 V, a very large current would flow that in many transistors might destroy the B-E junction. Electron flow from the emitter to the base is controlled by the voltage applied to the B-E junction.

With switch S open, no voltage is applied to the collector, and the collector does not affect the operation of the B-E junction. When S is closed, however, a large positive voltage (9 V in this case) is applied to the collector making the collector region of the transistor much more positive than the base region. This places a reverse bias on the B-C junction, and the B-C depletion layer becomes wide. We do not expect a current to flow across the B-C junction because of the scarcity of charge carriers in the B-C depletion layer. We find, however, that a large current does flow across this junction. Why?

The base region is physically very thin and is lightly doped with impurities in comparison with the emitter and collector. These factors reduce the total number of holes in the base region. When the B-E junction is forward biased, more electrons cross the B-E interface than there are holes in the P-type base region for them to

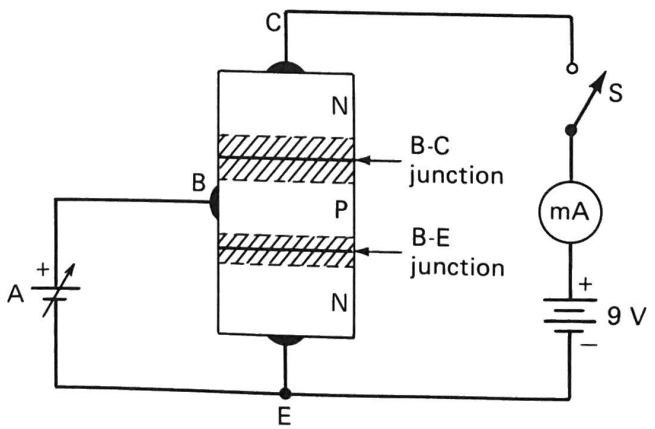


FIGURE 2-11 Battery A forward-biases the B-E junction. When switch S is closed, a collector current flows even though the B-C junction is reverse-biased.

drop into. Electrons "pile up" at the base edge of the B-E depletion layer, and this pile of electrons extends across the thin base region to the base edge of the B-C depletion layer. But the pile of electrons is not of equal depth across the base region.

In other words, the positive voltage applied to the base pulls electrons from the emitter into the base region. A small part of these electrons combine with holes in the *P*-type base material, but most remain in the base region as free electrons. The electron concentration is greatest near the B-E junction; it becomes smaller with increasing distance from the B-E junction and becomes nearly zero at the B-C depletion layer. This is illustrated in Figure 2-12.

The effect of this electron concentration *gradient* is to produce a *diffusion current* of electrons from the region of greatest electron concentration to the region of lower concentration. This produces a current flow from the emitter side to the collector side of the base region.

Recall that a wide depletion layer appears between the base and the collector regions that acts as an insulator due to the scarcity of charge carriers within the layer. The diffusion current serves to inject free electrons into the B-C depletion layer, and the injected electrons are readily drawn across the region to the collector. These electrons ultimately form the collector current in the external circuit.

Thus, a large current flows from the emitter to the collector of the transistor, and this current is under the control of the voltage applied to the base, or equivalently, the collector current is determined by the forward bias applied to the B-E junction. When the forward bias is increased, more electrons are drawn into the base region, the electron concentration gradient is increased, the diffusion current increases, and the collector current increases. The opposite effects occur when the forward bias of the B-E junction is decreased.

If the forward bias is removed from the base, no electrons will be drawn into the base region and no diffusion current will occur. Consequently, the collector current will be zero. Even if the collector is operated at a high voltage (less than the breakdown voltage of the transistor), no appreciable collector current will flow because the collector is not able to extract electrons from the emitter without assistance from the base.

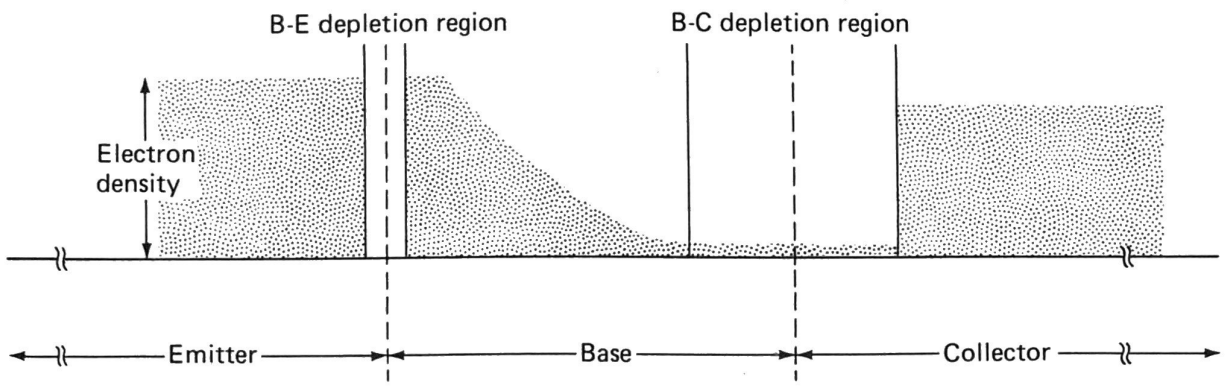


FIGURE 2-12 Electron densities in an *NPN* transistor. Electrons are most dense in the emitter, and somewhat less dense in the collector. The uneven density in the base region produces a diffusion current that introduces electrons into the depletion layer between the base and collector.

Current Gain from Base to Collector

Of the total number of electrons entering the base from the emitter, a small fraction (about 1%) will combine with holes in the base and be removed from the diffusion current. It is these electrons that combine with holes that ultimately constitute the current that flows from the base terminal of the transistor. In practice, it is desirable for the base current to be minimized.

Here is the principle that makes the transistor useful as an amplifier. A small base current, resulting from a voltage applied to the base, can effectively control a much larger current that flows from the emitter to the collector. In terms of energy, the base uses a small amount of energy to control a much greater expenditure of energy in the collector circuit. This is the principle on which amplification is based.

For a given transistor, there is an almost constant relationship between the base current I_b and collector current I_c. To a good approximation, the collector current is a constant multiple of the base current:

$$I_c = \beta I_b \tag{2-2}$$

The factor β is called the *beta* of the transistor, defined as the ratio of collector current to base current:

$$\beta = \frac{I_c}{I_b} \tag{2-3}$$

Typical values of β range from about 20 to 200 for transistors commonly encountered. The division of emitter current between the base and collector is illustrated in Figure 2-13.

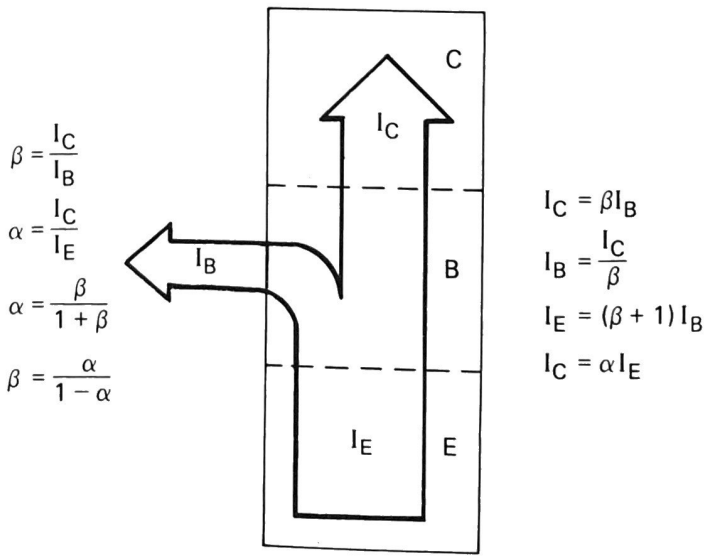
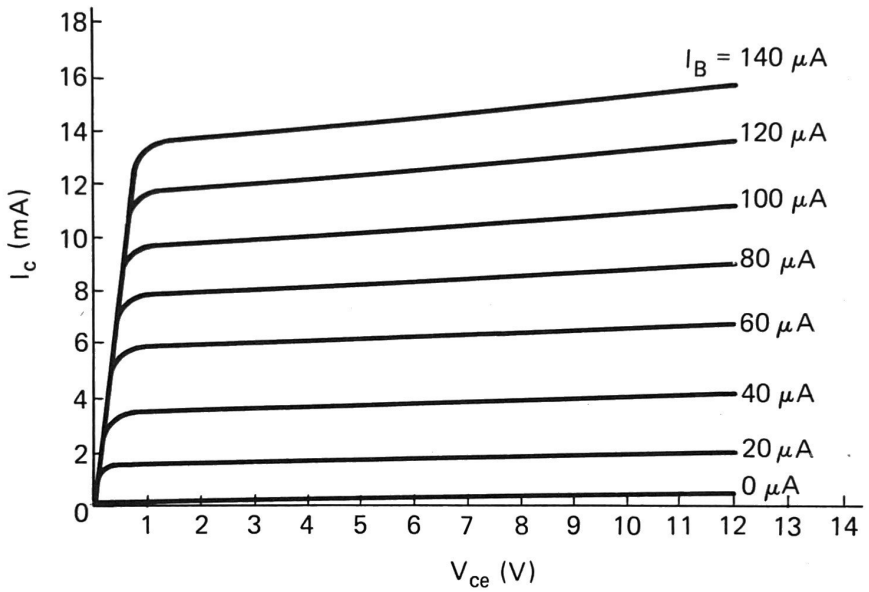


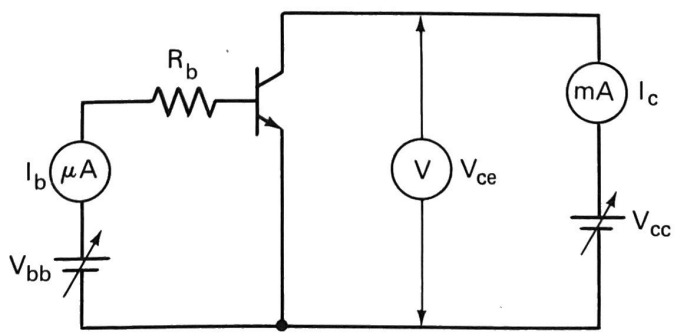
FIGURE 2-13 Illustration of the meaning of alpha (α) and beta (β), and applicable mathematical relationships.

Another parameter, besides beta, that relates to the division of emitter current between the base and collector is *alpha*, α. Alpha is the fraction of the emitter current that flows on to the collector. Its value is related to beta, as shown in Figure 2-13. Typical values of α range from about 0.95, a low value, to very nearly 1.0. Because alpha and beta are related so that one may be obtained from the other, alpha is seldom specified for a transistor; beta is the parameter most commonly encountered.

The operating characteristics of a typical transistor are shown in the graph of Figure 2-14(a), and the circuit used to obtain the curves is shown in part (b) of the figure. Voltage source V_{bb} is adjusted to give the desired base current I_b. Then source V_{cc} is varied to give the desired value of V_{ce} while the resulting value of I_c is recorded. (Curve tracers are available that display these curves automatically on the screen of a CRT.)



(a)



(b)

FIGURE 2-14 (a) Typical transistor characteristic curves. (b) Circuit used to obtain the curves.

Note that I_c increases sharply as V_{ce} is increased from zero. But when V_{ce} reaches about 0.2 V, the I_c curve flattens out and increases only slightly as V_{ce} becomes larger. The two regions are called the *saturation region* and the *linear region*, as indicated. In the linear region, V_{ce} is large enough so that the entirety (almost) of the base diffusion current is "collected" by the collector, and because the magnitude of this current is controlled by I_b, I_c increases only slightly with V_{ce}. In the saturation region, however, V_{ce} is not large enough to pull all the diffusion current into the collector.

2-6 JUNCTION FIELD-EFFECT TRANSISTORS

Another type of transistor is the *field-effect transistor* (FET) which works on an entirely different principle from that of the bipolar junction transistor (BJT) described in the previous sections. The family of field-effect transistors is shown in Figure 2-15. The type of FET that we shall describe first is the junction field-effect transistor, the JFET.

Junction FET (JFET)

Figure 2-16 shows a model of an N-channel JFET that illustrates the principle of operation. Actual device geometries differ greatly from this simple model, but the operating principles are the same. A bar of *N*-type material has *P*-type regions embedded on each side. *PN* junctions form where the two types of material meet, and the depletion layers extend into the interior of the bar as indicated. Contact is made to the side regions to form the third contact of the device, called the *gate*. The contacts to the ends of the bar are the *source* and the *drain*, as noted in the figure.

A current flows through the bar when a voltage is applied as shown in Figure 2-17. The resistance of the bar limits the current. The distribution of current is not uniform over the cross section of the bar, however, because the depletion regions formed around the gate junctions are depleted of charge carriers. Current flow can occur only through the interior portion of the bar, called the *channel*, between the

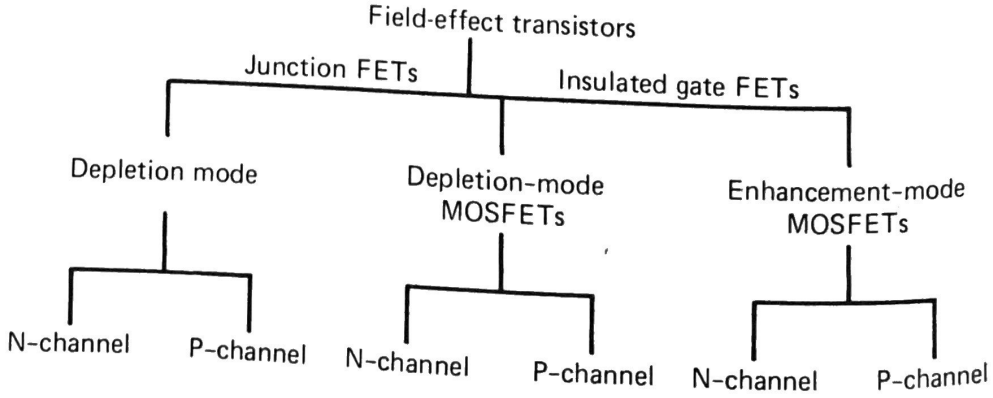


FIGURE 2-15 Family of field-effect transistors.

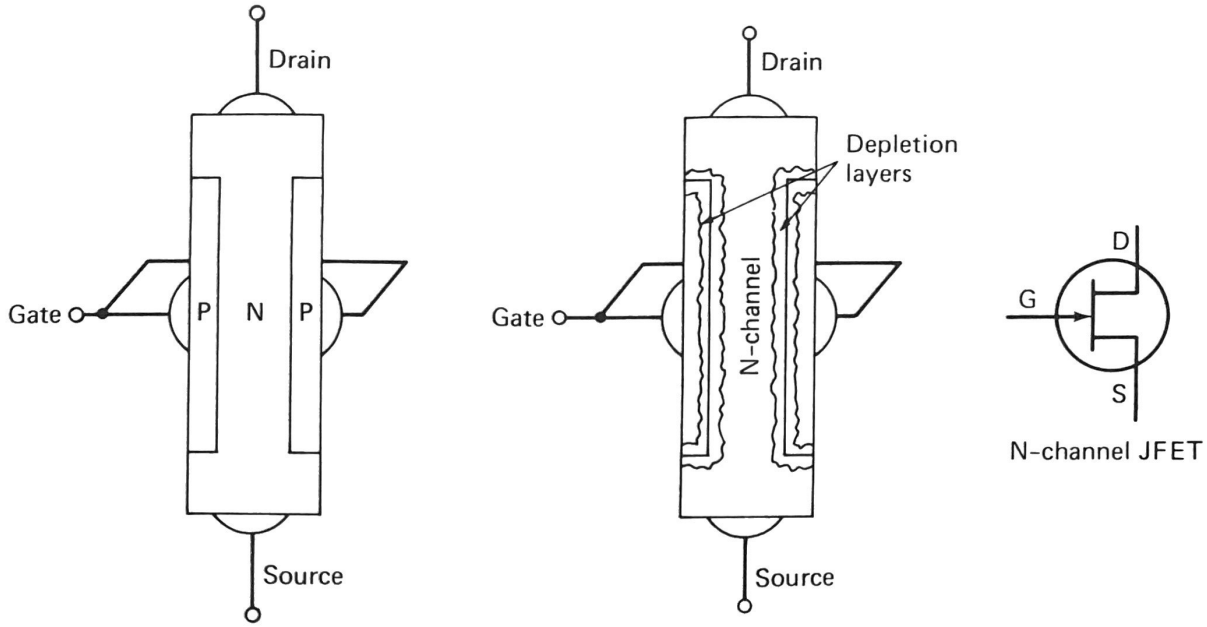


FIGURE 2-16 Model of a junction field-effect transistor (JFET). Depletion layers form at the junctions between the gate and the channel materials.

opposing depletion layers. The current that flows from the source through the channel to the drain is called the *drain current.*

We now consider the effect of a voltage applied to the gate upon the width of the depletion layers extending into the channel. By applying a voltage to the gate (relative to the source) that reverse biases the *PN* junctions, the width of the depletion layers can be made to vary as in an ordinary *PN* junction under the influence of a varying reverse bias. As the reverse bias is increased, the depletion layers extend farther into the channel, reducing its cross-sectional area. Since the

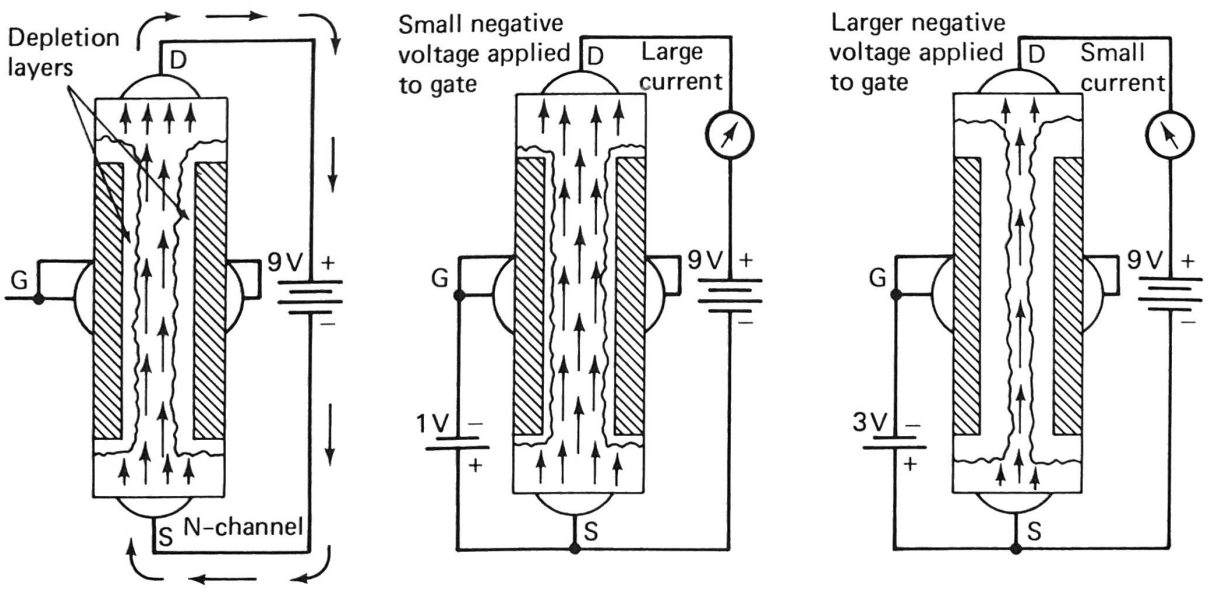


FIGURE 2-17 Dimension of the conductive portion of the channel depends upon the voltage applied to the gate. The gate voltage controls the width of the depletion layers.

resistance of the channel is determined, in part, by the cross-sectional area of the channel, the current flowing from the source to the drain due to the application of the drain voltage can be made to vary.

As the reverse bias at the gate is increased, the widening depletion layers cause the channel to shrink in cross-sectional area producing a decrease in the drain current. As the reverse bias is diminished, the cross-sectional area increases and so does the drain current. Thus, the voltage applied to the gate controls the drain current. This is the operating principle of JFETs.

Many details remain to be investigated, however. Since no current flows through the gate, all parts of the gate region are at the same voltage. This is not the case for the channel, because the drain current flows through the channel, and the drain-source voltage is distributed along the length of the channel. Consequently, the reverse bias of the gate-channel junction also varies along the length of the channel. As the reverse bias varies, so does the width of the depletion layers. The net effect is that the width of the depletion layers increases, proceeding from the source to the drain, causing the cross-sectional area of the channel to decrease. This condition is shown in Figure 2-18.

By applying sufficient reverse bias to the gate, it is possible to cause the depletion layers to come together to "pinch off" the conducting channel, and the voltage at which this occurs is called the *pinch-off voltage*. One might expect the drain current to vanish entirely at this point, but this does not happen, even though the drain current is significantly reduced. Although the depletion layers appear to touch at the center of the channel, a small region remains between the layers through which a concentrated stream of electrons flow to maintain the drain current. If the reverse bias is increased, more of the channel is pinched off and the current is further

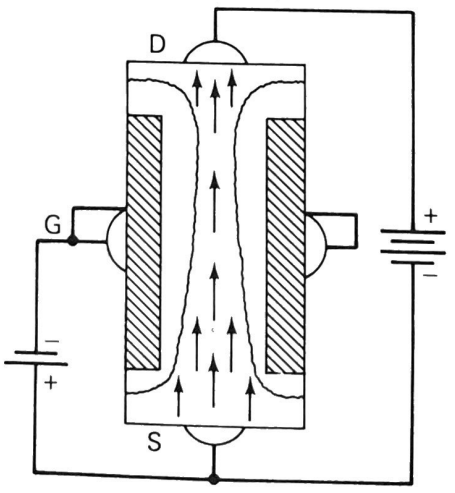


FIGURE 2-18 Width of the depletion layers is not uniform in a JFET because of the voltage variation along the length of the channel. The channel voltage is greater near the drain than at the source.

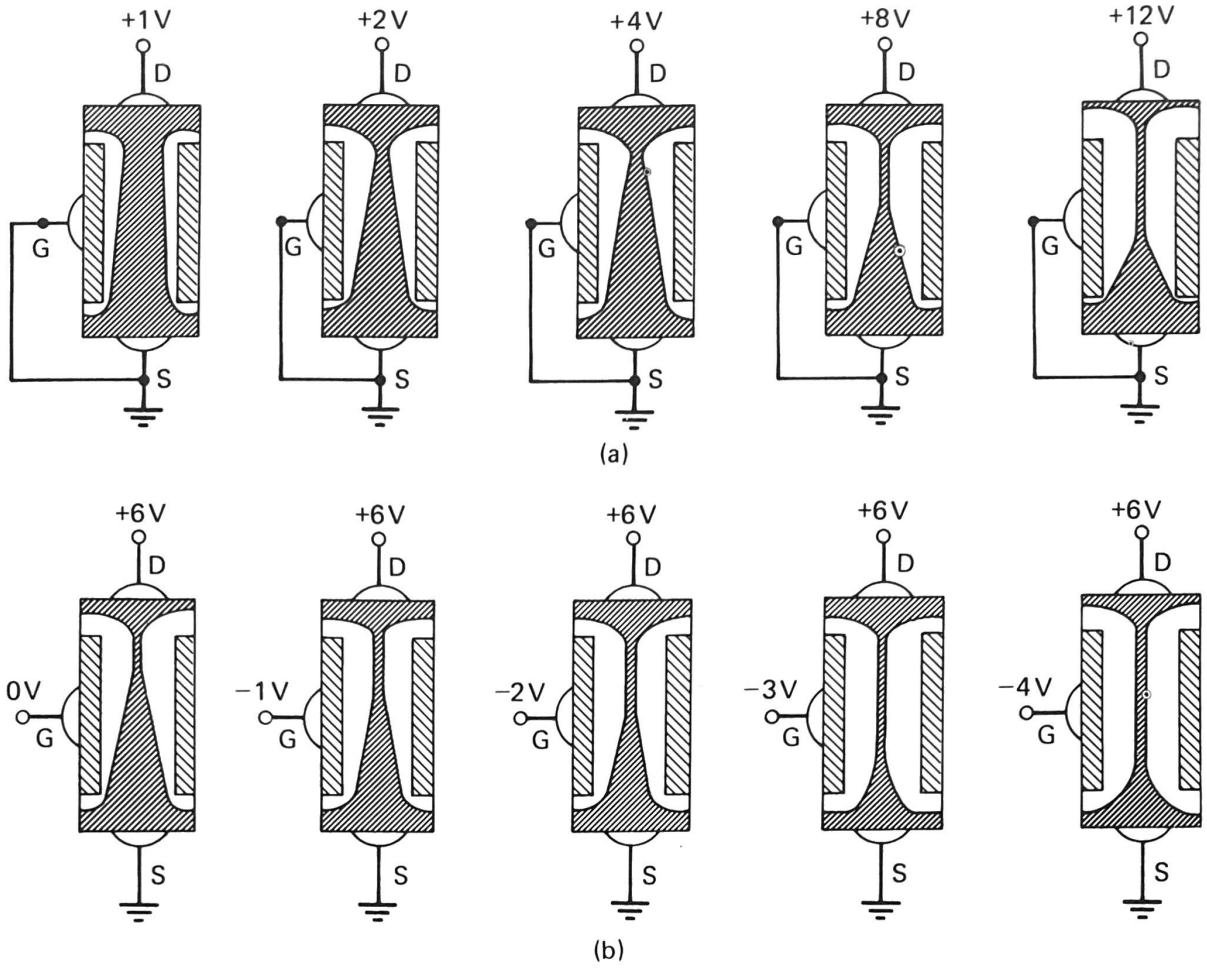


FIGURE 2-19 (a) Pinching off of the channel that occurs due to an increase in drain voltage. (b) Pinching off of the channel due to the application of a gate voltage.

decreased, but a current flow will still exist. By increasing the reverse bias still more, it is possible to reduce to negligible proportions the current flow from source to drain. Figure 2-19 illustrates the pinching-off action as the reverse bias is increased.

Drain Characteristics

Figure 2-20 shows the drain characteristics of a junction FET. At a given bias voltage, the graph of drain current versus drain voltage rises linearly at low values of drain voltage, where the channel acts almost as a resistor of constant value. At higher drain voltages, the graph begins to flatten out as the depletion layers decrease the width of the channel. When the drain voltage increases to the point where the reverse bias near the drain is just sufficient to pinch off the channel, the curve becomes essentially flat and remains so. The region of linear increase is called the *ohmic region* of the curve, and the flat portion is called the *saturation region*. In light of the saturation region of the drain characteristics, we say that a FET exhibits a constant-drain-current characteristic.

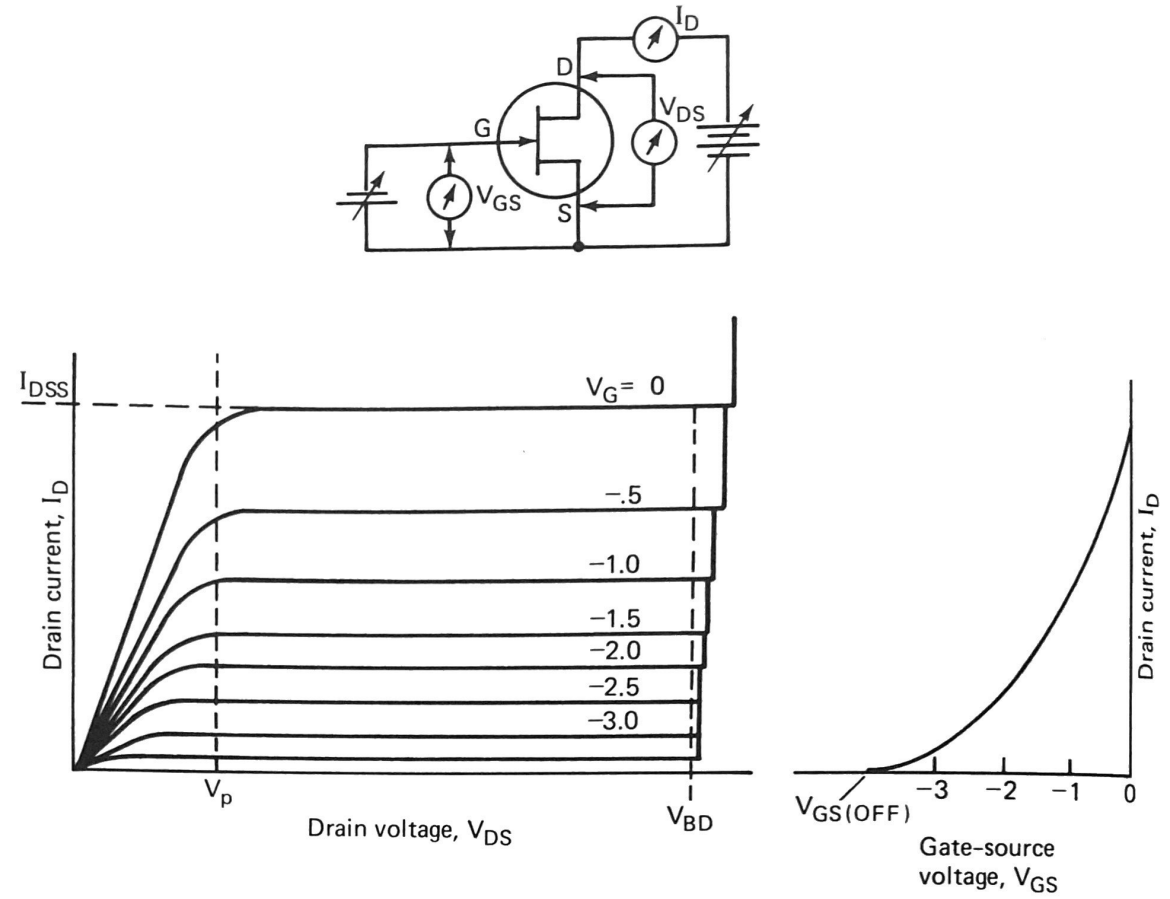


FIGURE 2-20 Typical drain characteristics and a typical transfer curve for an *N*-channel JFET.

To understand why the drain current does not continually increase with drain voltage, consideration must be given to two factors: (1) as the drain voltage is increased, a greater force is exerted on the electrons (in *n*-channel devices) to pull them through the channel from source to drain; (2) as the drain voltage is increased, the channel voltage near the drain is increased, and this produces a greater reverse bias on the *PN* junctions near the drain. This, in turn, reduces the conductivity of the channel as a result of the increased length of the pinched-off region.

These two effects are opposing forces that tend, for the most part, to cancel. As the drain voltage increases, the resistance of the channel increases almost proportionally, and the current flowing through the channel remains almost constant. This is illustrated in Figure 2-21.

Notable features of the drain characteristics include the pinch-off voltage V_p, the drain-source current with the gate shorted to the source I_{DSS}, and the gate-source cutoff voltage $V_{GS(off)}$. Also important is the breakdown voltage V_{BD} which, if exceeded, may lead to destruction of the device. JFETs are normally operated in the region of the characteristics between V_p and V_{BD}, where the characteristics are essentially flat. Note that the transfer characteristic resembles one-half of a parabola; this is called a *square-law response*, and the transfer curve of FETs follows the square law almost perfectly.

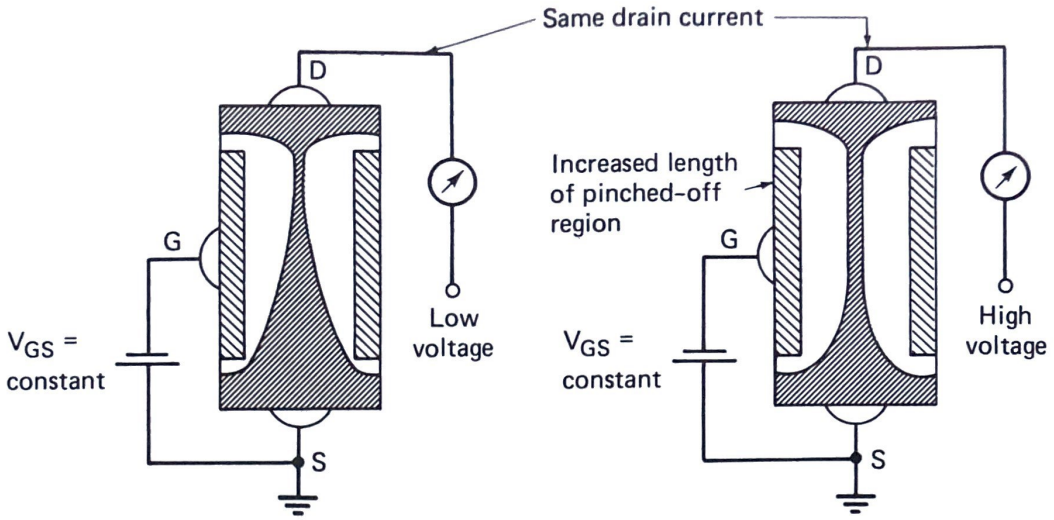


FIGURE 2-21 Increasing the drain voltage does not significantly increase the drain current because more of the channel is pinched off at high drain voltages.

Channel Material

Either *N*- or *P*-type material may be used as the channel of an FET, with the gate material always being of the opposite type. *N*-type materials have greater conductivity than *P*-type materials for the same impurity concentration, but it is sometimes advantageous to fabricate or use a *P*-channel device. Thus, both types are commonly encountered. The symbol for a FET indicates the type material used for the channel, and the symbols for both types are indicated in Figure 2-22.

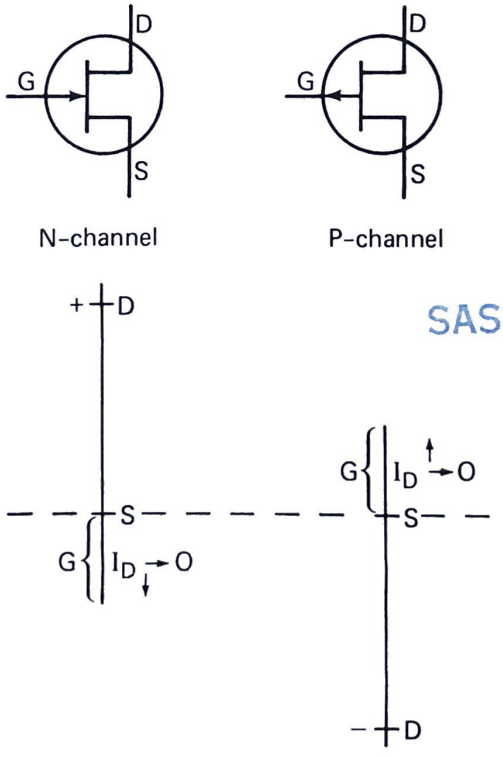


FIGURE 2-22 Symbols and biasing requirements for *N*- and *P*-channel junction field-effect transistors.

DC Voltage Polarities

In operation, the gate of JFETs is always reverse-biased. Hence, if the channel is *N*-type, the gate must be *P*-type, and the gate must be biased negative relative to the source. For an *N*-channel JFET, the drain is held positive relative to the source, and the gate is made more negative in order to reduce the drain current to zero. For a *P*-channel JFET, the drain is held negative relative to the source, and the gate is made more positive in order to reduce the drain current to zero. The biasing polarities are illustrated in Figure 2-22.

2-7 INSULATED GATE FETs—MOSFETs

Insulated gate FETs make use of the fact that a physical *PN* junction is not required to alter the conduction characteristics of the channel. The basic structure of this type of FET is shown in Figure 2-23, where it may be noted that the metal gate electrode is separated from the channel by a thin layer of insulating oxide. A voltage applied to the gate sets up an electric field that alters the availability of charge carriers in the channel. The acronym MOSFET identifies this type of FET, the metal-oxide-semiconductor field-effect transistor. MOSFETs may be either *N*-channel or *P*-channel, and we shall see that for each type of channel there are two modes of operation, the depletion mode and the enhancement mode.

Referring to Figure 2-24, note that a channel of *N*-type material is formed just underneath the insulating oxide opposite the gate electrode. When a negative voltage is applied to the gate, the holes of the *P*-type substrate are drawn toward the gate and combine with some of the electrons of the *N*-channel. This decreases the channel thickness, and current conduction from source to drain is diminished. If however, the gate is made less negative or even positive, the holes are repelled by the gate, and the *N*-channel becomes thicker, increasing conduction between source and drain. In this manner the voltage applied to the gate controls the current flowing in the channel.

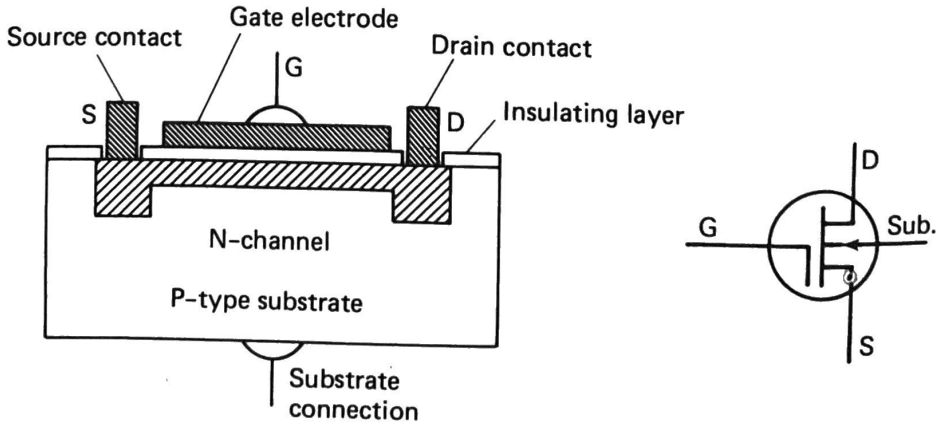


FIGURE 2-23 Structure and symbol for an *N*-channel depletion-mode MOSFET. Note that the gate is insulated from the channel.

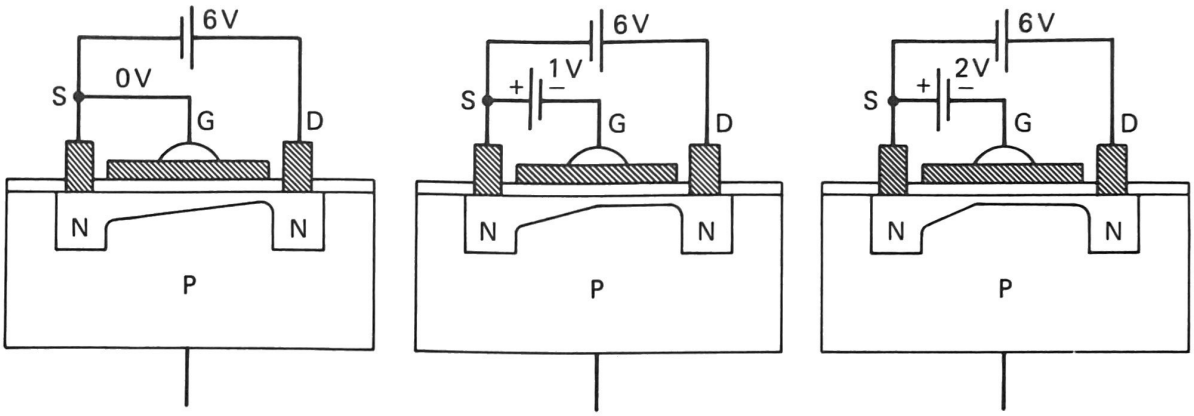


FIGURE 2-24 As the gate is made more negative, holes from the *P*-region are attracted into the *N*-channel, reducing its dimension. The pinching-off action is illustrated.

An important difference exists between this device and the junction FET described earlier. In the junction device the gate must always be reverse-biased relative to the channel to avoid a flow of current from the channel to the gate. In the MOSFET, however, the oxide layer provides the separation between the gate and the channel and no such restriction of the gate voltage exists.

Depletion and Enhancement Modes

The FETs discussed thus far exhibit near-maximum conduction with zero bias voltage applied to the gate. Application of a bias voltage causes a narrowing of the channel as the depletion layers become wider and conduction is diminished. Such devices are said to operate in the depletion mode because the bias voltage depletes the channel. We now come to a class of MOSFETs that exhibit minimum or near-zero conduction at zero bias. These devices require a bias voltage to produce source to drain conduction and are said to operate in the *enhancement mode*.

Figure 2-25 shows the structure of an *N*-channel enhancement-mode MOSFET; note the absence of a channel from source to drain. In order for the device to conduct, a channel must be *induced* by a positive voltage applied to the gate

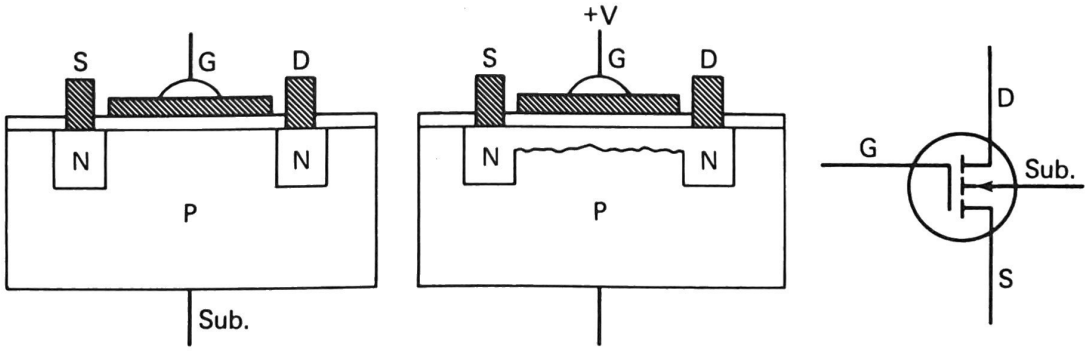


FIGURE 2-25 Structure and action of an *N*-channel enhancement-mode MOSFET. The gate must be made positive to induce a channel between the source and the drain.

electrode. A positive voltage on the gate attracts electrons to the vicinity of the gate and forms an effective *N*-channel. When the positive voltage is removed, the channel disappears and conduction through the device will cease. *P*-channel enhancement MOSFETs operate in a similar manner, where a negative voltage must be applied to the gate to attract holes in order to form a channel. The symbol for enhancement MOSFETs denotes the normally open channel by using a broken line to indicate the channel. This and a summary of the voltage polarities required for the different types of MOSFET's are given in Figure 2-26.

Substrate

The bottom supporting layer of planar-type semiconductor devices is called the *substrate*, and in many device geometries, an undesirable *PN* junction is formed between the substrate and the active portion of the device, as shown in Figure 2-27. This undesired junction must be kept reverse-biased in order to be electrically inactive. If the substrate becomes forward-biased relative to the channel, catastrophic failure of the device may result as large currents flow in the forward-biased *PN* junction. Many packages provide an external lead to the substrate which must

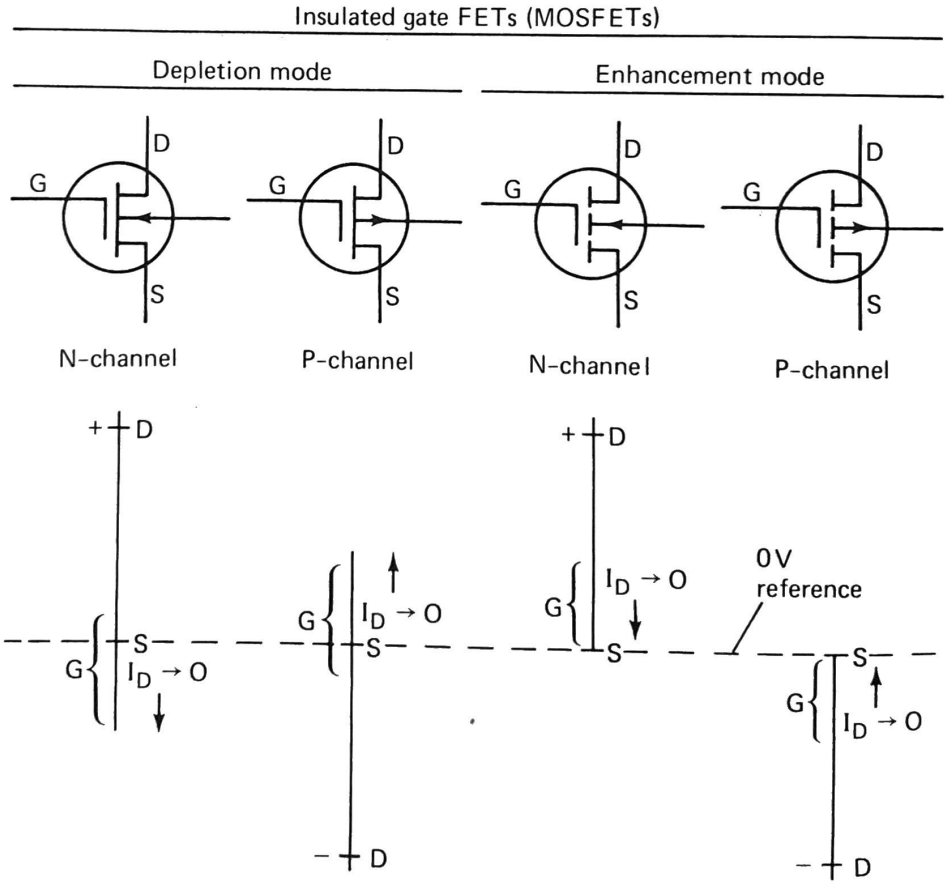


FIGURE 2-26 Symbols and biasing requirements of insulated gate FETs (MOSFETs). The region of allowed gate voltages is indicated, and the polarity of gate voltage required to reduce the drain current I_D to zero is shown.

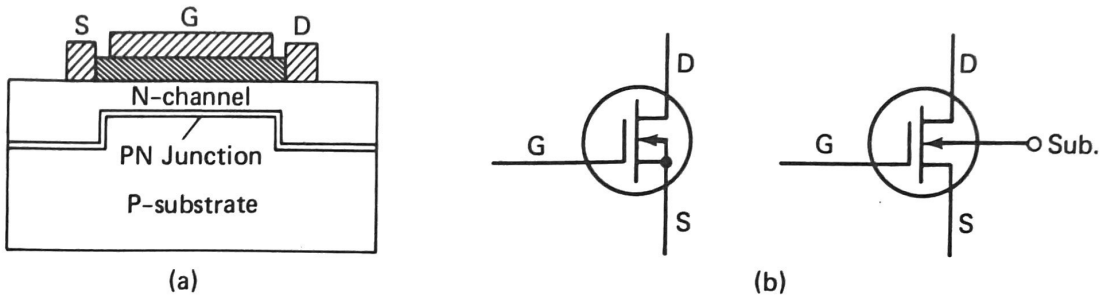


FIGURE 2-27 (a) A *PN* junction is formed between the channel and substrate of a MOSFET. (b) The substrate may be connected internally to the source or an external connection may be provided for the substrate.

be properly connected. For *P*-type substrates, the substrate is commonly connected to ground or to the most negative part of the circuit. In other devices the substrate is internally connected, with no external lead provided. For MOSFETs the substrate connection is shown on the symbol, as may be noted in Figure 2-27.

Dual-Gate MOSFETs

Figure 2-28 shows the structure of a dual-gate, depletion-mode, *N*-channel MOSFET. Note the source contact and the drain contact, and note that an extra region of *N*-type material divides the channel into two sections in series. Each section of the channel has a gate electrode, where the gates are identified as gate 1 and gate 2. Gate 1 is closest to the source. Each gate is capable of cutting off the current in its section, and therefore, either gate can cut off the flow of current through the entire device. Considering the device as two single gate devices in series, the device source serves as the source for section 1 while the central region serves as the drain. The central region, in addition to acting as a drain for section 1, serves as the source for section 2. The device drain serves as the drain for section 2.

The independent pair of gates makes the device applicable to RF amplifiers, gain-controlled amplifiers, mixers, demodulators, and so forth. As a controlled-

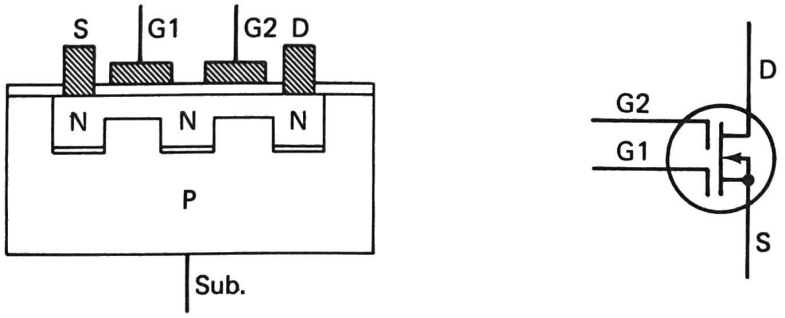


FIGURE 2-28 Structure and symbol of a dual-gate, *N*-channel, depletion-mode MOSFET. In the symbol, the substrate is shown connected internally to the source.

gain amplifier, the signal to be amplified is applied to gate 1 while a DC control voltage derived from an automatic-gain-control circuit is applied to gate 2. Also, the presence of the second gate section tends to isolate the device drain from the input signal applied to gate 1, and this allows high-frequency operation well into the UHF range without need of neutralization.

Handling MOSFETs

The gate electrode of a MOSFET is insulated from the channel region by an insulating layer of extremely high resistance. The insulating layer is so thin, however, that a voltage difference on the order of 100 V between the gate and the channel will cause the insulation to break down, giving rise to "punch-through" in which the gate is shorted to the channel, destroying the device.

Small charges of static electricity can easily develop sufficient gate-channel voltage to puncture the insulation. Such charges may come from fingertips, tools, soldering devices, plastic materials, Styrofoam, and so forth. It is possible to destroy a MOSFET simply by removing it from its package. Hence, special precautions must be taken when handling MOSFETs.

MOSFETs are shipped with all leads shorted, either by a metal spring, metal foil, or by a special conductive foam. If possible, metal springs or clips should not be removed until after the device is soldered into the circuit. If the conducting foam is used, it should not be removed until just before the device is inserted into the circuit, and then only after precautions against static electricity have been taken.

Precautionary measures include grounding the soldering device, the receiver chassis, and the technician. Insulating materials—plastic, rubber, nylon—are the most dangerous and should not be allowed to contact the device. A small piece of lightly moistened tissue may be wrapped around the device to short the leads during handling. Equal care is needed when removing a MOSFET from a circuit for testing.

Some MOSFETs are provided with internal protection diodes that limit the gate-channel voltage, but it is good practice to handle all MOSFET devices with special care.

2-8 OPERATIONAL AMPLIFIERS

Integrated circuit (IC) technology has provided a multitude of specialized devices in the form of "chips" so that it now seems that there is a chip for every chore. However, one category of linear IC that is definitely general purpose is that of the *operational amplifier*, the op amp. With only minor variations in the external circuitry, a general-purpose op amp can be made to perform a wide variety of functions. In this section we present the highlights of these devices. The symbol for a general-purpose op amp and the typical power supply connection are shown in Figure 2-29.

Typical features of a general-purpose op amp include: (1) two inputs, one inverting and one noninverting; (2) an input impedance of 1 MΩ or more; (3) an

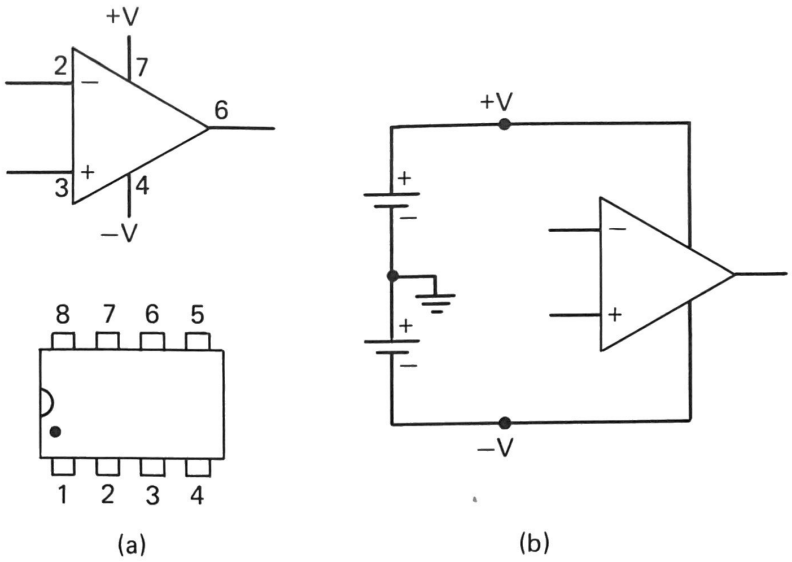


FIGURE 2-29 (a) Symbol and top view of a general-purpose op amp. The pin numbers are given for the familiar 741. (b) Connections for operation with a balanced power supply.

output impedance that typically is less than 100 Ω; and (4) a very large low-frequency gain, typically more than 100,000. Also, most op amps are intended to operate from a balanced power supply so that the output voltage may swing symmetrically above and below zero volts. Some op amps include an offset-null adjustment that permits the output voltage to be adjusted to exactly zero volts when the input voltage is zero.

Strictly speaking, the op amp is a difference amplifier; the output is a greatly amplified version of the *difference* in the voltages applied to the two inputs. A positive voltage applied to the noninverting (+) input drives the output to a more positive value, but a positive voltage applied to the inverting (−) input drives the output to a more negative value. The net output voltage is the difference of these two effects.

In practical applications, the very large gain (about 100,000) is reduced dramatically to usable levels by the use of *negative feedback*. A portion of the output voltage is brought back to the input side, where it is applied to the inverting input terminal. Then, when the output goes more positive, for example, the voltage applied to the inverting input will also go more positive. This will tend to drive the output toward the negative. Any movement of the output voltage will be counteracted (somewhat) by the voltage fed back to the inverting input terminal. The net effect is a reduction in gain of the overall amplifier.

Voltage Follower

An extreme case in which all the output voltage is fed back to the inverting input is represented by the *voltage follower*, shown in Figure 2-30. Suppose that a positive voltage of 1 V is applied to the (+) input, which represents the signal input for the circuit. This will drive the output voltage positive due to the large gain of the

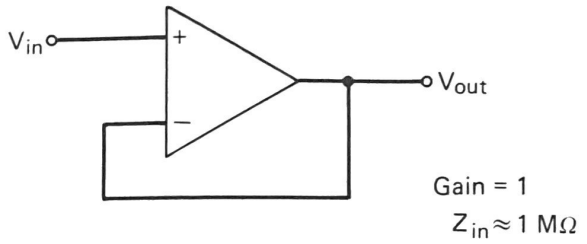


FIGURE 2-30 Voltage follower. The high input impedance and low output impedance makes this circuit useful as an impedance-matching device.

op amp itself. But when the output voltage reaches 1 V, the same voltage will be applied to the inverting input (via the feedback connection) and the output voltage will stabilize at 1 V. At this point, there will be (for practical purposes) zero differences in voltage between the two inputs. This condition of zero difference in voltage between the two inputs is a common feature of all op amp amplifier circuits.

Let us now examine the action of this circuit more closely, paying attention to some tiny voltages that were neglected in the above. Again, suppose that +1 V is applied to the (+) input. The output voltage will rise, but it will not rise all the way to 1 V, as we implied above. Instead, it will fall short of 1 V by about 1/100,000 V, which is 10 μV. (We are assuming the gain of the op amp to be 100,000.) Consequently, the voltage fed back to the (−) input will be 10 μV less than 1 V. This means that the difference in voltage between the (+) and (−) inputs will be 10 μV. Then, because an op amp is a difference amplifier, the 10-μV difference will be amplified by 100,000. This gives rise to the (very nearly) 1 V at the output.

From this we conclude that the gain of the voltage follower is 1; the output voltage is the same as the input voltage; or, the output voltage follows the input voltage. The usefulness of the circuit stems from its high input impedance (about 1 MΩ) and very low output impedance (< 100 Ω); it is used as a buffer amplifier or as an impedance-matching device.

Open-Loop and Closed-Loop Gain

The voltage gain exhibited by an op amp without feedback is called the *open-loop gain*, and it is very large, as we have seen. But as amplifiers, op amps are always operated with negative feedback in order to reduce the gain to useful levels. The negative feedback path closes the loop around the op amp itself, and we refer to the gain of the entire circuit as the *closed-loop gain*. For the voltage follower, the closed-loop gain is 1 while the open-loop gain is on the order of 100,000.

Noninverting Amplifier

When 100% of the output voltage V_{out} is fed back to the (−) input, we obtain a closed-loop gain of 1, that is, a voltage follower. If, however, only a fraction of V_{out} is fed back, we achieve a closed-loop gain greater than 1. A convenient way

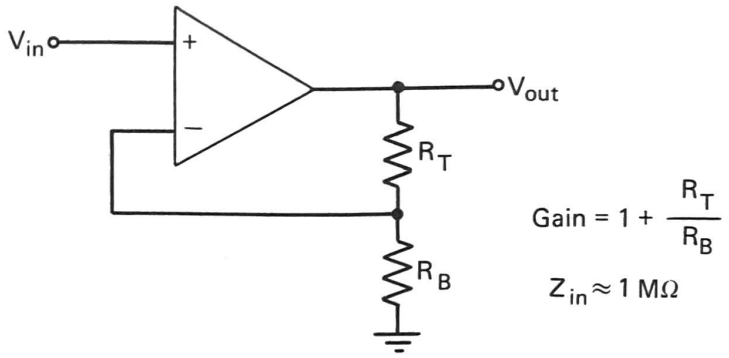


FIGURE 2-31 Noninverting amplifier. When R_T is 10 kΩ and R_B is 1 kΩ, the gain is 11.

to obtain the fraction of V_{out} is to use a voltage divider on the output, as shown in the schematic of Figure 2-31. The resulting amplifier is known as a *noninverting amplifier*.

Inverting Amplifier

Another amplifier, shown in Figure 2-32, has the input signal applied through R_s to the inverting input so that the output signal is inverted relative to the input signal. The net signal appearing at the (−) input is due to the combination of V_{in} applied through R_s, and V_{out} applied through R_f. Because V_{in} and V_{out} are inverted relative to each other, the two component voltages at the (−) input tend to cancel. Therefore, the voltage at the (−) input is always within a few tens of microvolts of zero, and the difference voltage is, accordingly, rather small. Because the (−) input is always at very nearly ground potential (the same as the (+) input), it is sometimes called a *virtual ground*. The closed-loop voltage gain is determined by the ratio R_f/R_s, and because of the virtual ground at the (−) input, the input impedance to the circuit is the same as R_s.

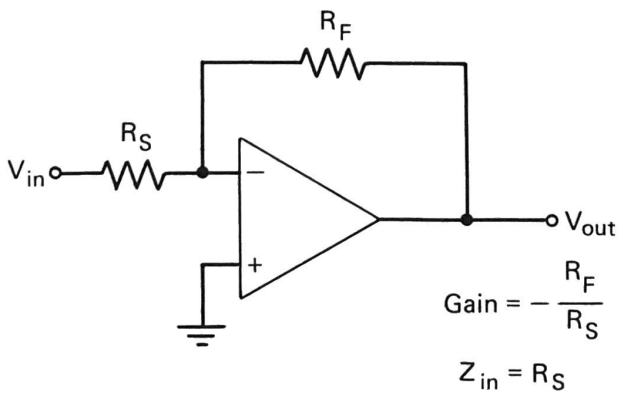


FIGURE 2-32 Inverting amplifier. The minus sign associated with the gain indicates that the output signal is inverted relative to the input signal.

Op Amp Limitations

Even though op amps are suitable for a wide range of applications, they suffer from at least three significant limitations. One is that their high-frequency response is rather limited. The open-loop gain drops off dramatically with increasing frequency. For example, an op amp having an open-loop gain of 100,000 at very low frequencies might have have a gain of only 100 at a frequency of 10 kHz, of 10 at 100 kHz, and of only 1 at 1 MHz. The *gain-bandwidth product* (GBW) expresses this property. If the GBW of an op amp is known, the expected open-loop gain A_{ol} at a frequency f is given by

$$A_{ol} = \frac{\text{GBW}}{f} \tag{2-4}$$

The GBW of a 741 general-purpose op amp, for example, is 1 MHz.

Another limitation arises from the fact that the output voltage cannot change instantaneously from one value to another. The rate at which the voltage changes is called the *slew rate*, and the maximum slew rate is an important op amp specification. For a 741, the maximum slew rate is 500,000 V/s, or 0.5 V/μs.

The maximum slew rate of a sine-wave voltage is given by

$$\text{SR}_{\text{max}} = 2\pi f V_p \tag{2-5}$$

where f is the frequency in hertz and V_p is the peak voltage of the sine wave. Note that SR_{max} depends on both the frequency and amplitude of the sine wave. You may verify that a 1-kHz sine wave whose peak amplitude is 10 V has a maximum slew rate of 62,832 V/s. This is well under the 500,000-V/s capability of a 741 op amp, which can reproduce the waveform with no difficulty.

The third limitation arises from the electrical noise produced within the device. In applications where very small signals are to be amplified, better results (signal/noise ratio) are usually obtained with discrete devices. However, special low-noise op amps can be obtained at a somewhat higher price that offer excellent noise characteristics.

2-9 THE VACUUM DIODE

The central structure of a vacuum tube is the *cathode*. It consists of a hollow, oxide-coated metal cylinder that surrounds an electric *heater* which heats it to red-hot temperatures. When heated, the cathode emits electrons from its outer surface, and a cloud of electrons forms around the cathode. The phenomenon of electron emission due to heat is called *thermionic emission*, and the electron cloud that forms around the cathode is called the *space charge*.

A *vacuum diode* is made by surrounding the cathode with a metal cylinder called the *anode*, or more commonly, the *plate*. When the plate is made more positive than the cathode, electrons flow from the cathode via the space charge to

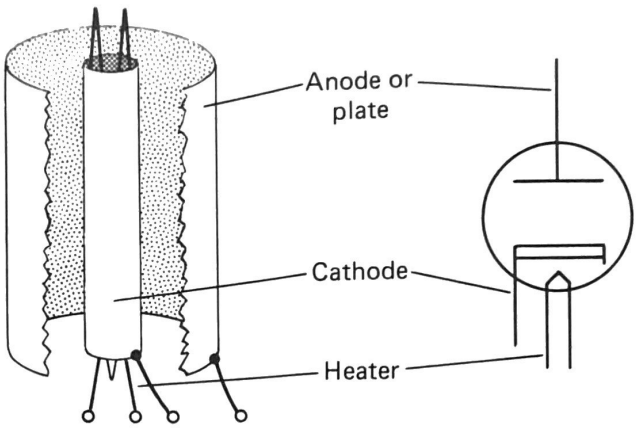


FIGURE 2-33 Structure and symbol for a vacuum diode.

the plate. That is, an electron current flows from the cathode to the plate. But when the cathode is made more positive than the plate, no current flows from the plate to the cathode because the plate is not heated to temperatures sufficiently high for it to emit electrons. Thus, electrons will flow from the cathode to the plate, but they will not flow from the plate to the cathode. The device exhibits the property of a rectifier; its structure and schematic symbol are shown in Figure 2-33.

The Triode

Control over the electron current flowing from the cathode to the plate can be achieved by surrounding the cathode with a loosely wound spiral of thin wire, called the *grid*. When the grid is made negative relative to the cathode, the plate current becomes smaller. This happens because the electrons of the space charge are repelled by the negative charge on the grid. Conversely, the plate current increases when the grid becomes less negative. This ability of the grid voltage to control the plate current makes the *triode* (as the device is called) useful as an amplifier. The structure and schematic symbol of a triode are shown in Figure 2-34.

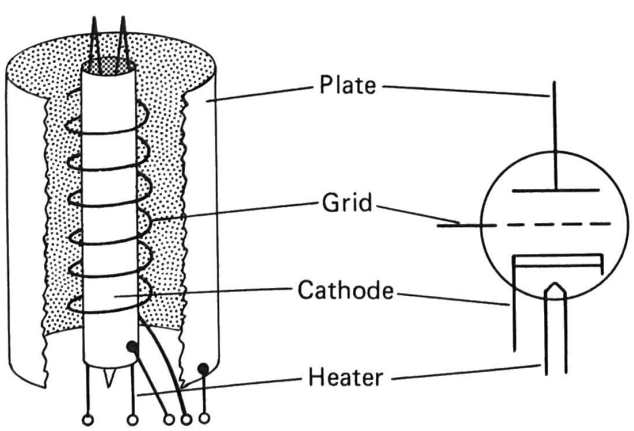


FIGURE 2-34 Structure and symbol for a vacuum triode.

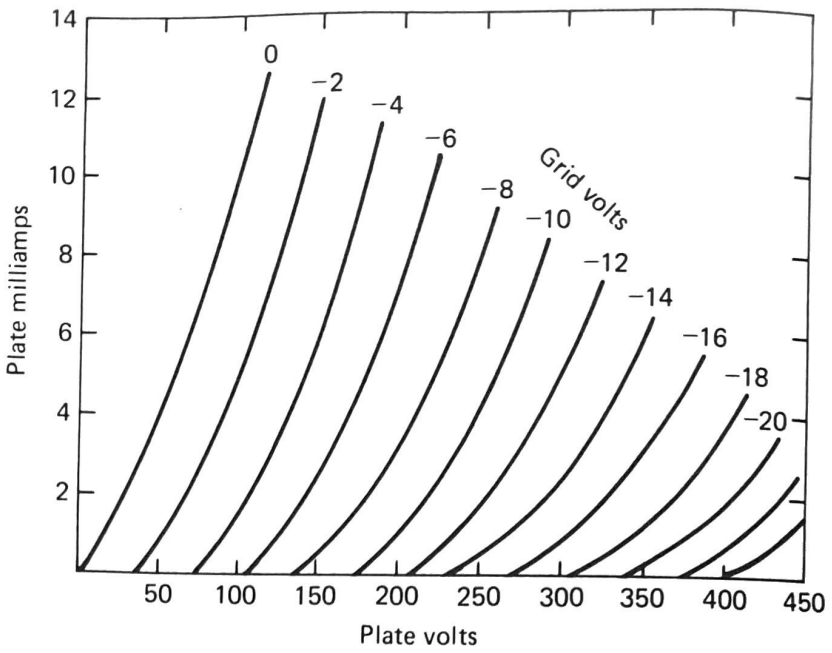


FIGURE 2-35 Plate characteristics of a triode.

Plate Characteristics of a Triode

The performance characteristics of a triode are given by its plate characteristics. The plate characteristics of a typical triode are shown in Figure 2-35. The grid curves illustrate the effect of the grid voltage in controlling the plate current. Note that for a given plate voltage, a larger and more negative grid voltage reduces the plate current. In the figure, for a plate voltage of 150 V, about 6 mA of plate current flows when the grid is -4 V with respect to the cathode, and only about 2 mA flows when the grid is held at -6 V.

SUMMARY

1. The minute conductivity of intrinsic (pure) silicon or germanium is due to thermally induced electron-hole pairs that give rise to free electrons and free holes. The conductivity increases with temperature as more electron-hole pairs are produced.
2. A movement of holes to the left is equivalent to, and in fact is caused by, a movement of electrons to the right. A hole moves by virtue of a succession of electron jumps in the opposite direction.
3. The *N*-type impurities, phosphorus, arsenic, antimony, and bismuth, have five electrons in their outer shell and contribute free electrons to the semiconductor. The *P*-type impurities, aluminum, boron, gallium, and indium, have only three electrons in their outer shell and contribute free holes to the semiconductor.

4. A depletion layer forms at the interface of a *PN* junction due to the passage of free electrons from the *N*-side to the *P*-side, where they combine with free holes. The depletion layer may be regarded as a layer of insulation because the free electrons and holes in the layer have been depleted.

5. When a *PN* junction is forward biased (by making the *P*-material positive relative to the *N*-material), the depletion layer becomes thinner and a large current will flow. Under reverse bias, the depletion layer becomes thicker, and only a very small leakage current will flow.

6. *PN* junctions (solid-state diodes) serve as rectifiers in power supplies for converting AC to DC. Zener diodes have a very sharp reverse breakdown characteristic and are used as voltage regulators. Light-emitting diodes (LEDs) are widely used as indicator lamps.

7. About 0.7 V is required to forward bias a silicon diode, but only about 0.25 V is required to forward bias a germanium diode. An LED requires about 1.7 V to forward bias it to the conduction region.

8. The B-E junction of a bipolar junction transistor is forward-biased in normal operation. Current flows across the base region by a process of diffusion.

9. Fundamentally, a BJT is a current multiplier: the base current is multiplied by the beta of the transistor to yield the collector current. The base current is controlled by the voltage applied to the B-E junction.

10. In the linear region, the collector current increases only slightly as the collector voltage is increased.

11. The terminals of a BJT are the emitter, base, and collector. These correspond to the source, gate, and drain of a FET, and to the cathode, grid, and plate of a vacuum triode.

12. Whereas the B-E junction of a BJT is forward-biased, the gate-channel junction of a JFET is always reverse-biased.

13. Current flow from the source to the drain of a JFET is controlled by the dimensions of the channel, which, in turn, are controlled by the voltage appearing between the gate and source.

14. The biasing requirements of an *NPN* transistor, *N*-channel JFET, and vacuum triode are similar in that the collector, drain, or plate is held positive relative to the emitter, source, or cathode.

15. In a MOSFET, the gate electrode is completely insulated from the channel by a layer of oxide. Consequently, the gate voltage may be of either polarity relative to the source, and this makes it possible to fabricate both depletion-mode and enhancement-mode MOSFETs.

16. Conduction from source to drain occurs normally and naturally in a depletion-mode FET; a voltage must be applied to the gate to reduce the level of conduction. In enhancement-mode FETs, however, no conduction will occur until a voltage applied to the gate causes it to occur.

17. The gate-channel junction of a JFET must never become forward-biased. Therefore, the gate voltage of a JFET is restricted to one polarity. In MOSFET devices, however,

no such restriction exists. Consequently, MOSFETs occur of both depletion-mode and enhancement-mode types.

18. Dual-gate MOSFETs have two gates, which makes the devices useful as controlled-gain RF amplifiers, mixers, demodulators, and so on.

19. Special care is needed in handling MOSFET devices because static discharges can easily destroy the device by puncturing the insulation between the gate and the channel.

20. An operational amplifier is a very high gain general-purpose amplifier that may be tailored to a wide variety of application by adding a few external components. It is a difference amplifier. Negative feedback is used to reduce the gain to practical levels.

21. A voltage follower, which uses 100% negative feedback to reduce the circuit gain to unity, is often used as an impedence-matching device.

22. A noninverting op amp amplifier may utilize a voltage divider to return only a fraction of the output signal voltage back to the input as negative feedback.

23. An inverting op amp amplifier incorporates resistances in series with the input signal path and in series with the feedback path from output to input.

24. Op amp limitations include a limited high-frequency response, a limited slew-rate capability, and a tendency to produce greater amounts of electrical noise than amplifiers using discrete components.

25. A vacuum diode consists of a cathode, a plate, and a heater inside the cathode to heat the cathode to temperatures at which thermionic emission will occur.

26. A triode includes a grid situated between the cathode and plate. Making the grid more negative reduces electron flow from the cathode to the plate.

QUESTIONS AND PROBLEMS

2-1. What is an electron-hole pair? Why do free electrons and holes occur in pairs in intrinsic semiconductors? What is responsible for the generation of electron-hole pairs?

2-2. Describe the mechanism by which the presence of electron-hole pairs increases the electrical conductivity of a semiconductor.

2-3. Why does a hole appear to have a positive charge even though a hole is really nothing?

2-4. Explain why the presence of holes in a *P*-type semiconductor increases the electrical conductivity of the material.

2-5. What are the majority and the minority carriers in *N*-type semiconductor material?

2-6. What causes a depletion layer to form at the interface between the *N* and *P* regions of a *PN* junction?

2-7. What happens to the depletion layer when a *PN* junction is forward biased?

2-8. When a *PN* junction made of silicon is forward-biased, what approximate voltage appears across the junction under conditions of moderate conduction?

2-9. Describe the reverse-breakdown characteristic of a zener diode. What is the primary application of zener diodes?

2-10. In normal operation of an *NPN* transistor, what voltage polarities are applied to the base and collector regions? Which is more positive?

2-11. Why is it necessary to forward-bias the B-E junction?

2-12. In normal operation the B-C junction of a BJT is reverse-biased, yet a large current easily flows across the junction. What is responsible for this effect?

2-13. Why do most of the electrons entering the base region go on to the collector?

2-14. A transistor is often called a current multiplier. What current is multiplied? What is the beta of a transistor?

2-15. How do the emitter and collector currents compare? How does the base current compare with the collector current?

2-16. In normal operation of a BJT, the collector current is controlled by the voltage existing between which two elements of the transistor?

2-17. Explain how the structure of a JFET differs from that of a BJT.

2-18. Why must the gate-channel junction of a JFET always be reverse-biased?

2-19. Why are there no enhancement-mode JFETs?

2-20. To reduce the drain current of an *N*-channel JFET, should the gate voltage be made more positive or more negative?

2-21. In normal operation, should the gate of a *P*-channel JFET be positive or negative relative to the source?

2-22. How does the structure of a MOSFET differ from that of a JFET?

2-23. With the gate terminal shorted to the source of an *N*-channel device, will any drain current flow when a moderate voltage (say, 6 V) is applied between the drain and source:

(a) of a JFET?

(b) Of a depletion-mode MOSFET?

(c) Of an enhancement-mode MOSFET?

2-24. The channel-substrate junction of MOSFETs must always be reverse-biased. Why?

2-25. To stimulate an enhancement-mode, *N*-channel MOSFET into conduction, must the gate be made positive or negative relative to the source?

2-26. Why must MOSFETs be handled carefully in regard to static electricity?

2-27. What does it mean when we say that op amp is a difference amplifier?

2-28. What technique or principle is used to reduce the large, open-loop gain of an op amp to practical levels?

2-29. Why are most general-purpose op amps operated from a balanced power supply?

2-30. Describe the three major limitations of op amps.

2-31. In a vacuum diode, why will electrons not flow from the plate to the cathode even when the cathode is made positive relative to the plate?

2-32. Does the plate current of a vacuum triode increase or decrease as the grid is made more negative?

2-33. In normal operation, is the grid voltage of a triode held negative or positive relative to the cathode?